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Sigma Delta Modulator Based Multi-Standard Transmitter Design For Wireless Communication Applications

By

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Abstract:

This paper presents a sigma delta modulator (ΣΔM) based transmitter that is suitable for digital multi-standard wireless applications especially for software defined radio (SDR) systems. The proposed transmitter mainly consists of a sigma-delta modulator and a switching-mode power amplifier. In the proposed design, a third order low-pass ΣΔM is implemented to produce a high frequency digital-like signals that is used to drive a high efficient class-E switching mode power amplifier. The target technology for fabrication is TSMC180nm CMOS process. The proposed design is tested for different standards such as Global System for Mobile Communications (GSM), Universal Mobile Telecommunications System (UMTS), Wi-Fi and Long Term Evolution (LTE) with frequency bands of (1.8GHz, 2.1GHz, 2.4GHz, (1.9, 2.6GHz)) respectively. The class-E power amplifier has shown peak power added efficiency (PAE) and peak output power of 62/58.7/60/52/47% and 27.7/27.5/27.6/27/26.7dBm, respectively, at the mentioned standards. Moreover, the proposed power amplifier can cover a wide range of frequency from 1.8GHz to 2.6GHz maintaining high efficiency.

Keywords:

RF digital transmitter, sigma-delta modulator (ΣΔM), class-E power amplifier

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1. Introduction:

The rapid growth in wireless communication standards is evolving towards high data rate, multiband, multimode, multi-standard, low power radio communication, higher signal-to-noise ratio, low-cost, and flexible system. Software defined radio (SDR) becomes the solution to improve the interoperability between different wireless standard [1].

Software-defined radio (SDR) is a radio communication technology that is based on software defined wireless communication protocols instead of hardwired implementations. In other words, frequency band and functionality can be upgraded with software download and update instead of a complete hardware replacement. This flexibility allows the SDR system to work for different existing wireless standards. It can also be easily upgraded for upcoming standards, with only the need to update the software [2].

Typical digital input/RF output SDR transceivers are composed of a digital signal processing (DSP) component and an RF component as shown in Figure (1). Generally, the RF transmitter part includes digital-to-analog converters, a frequency up-conversion stage, and a power amplifier (PA) [3].

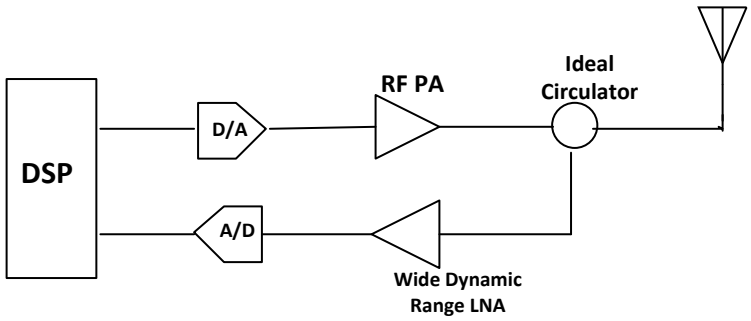

Figure (1): *Ideal software SDR transceiver architecture*

In practice, the input signal of the PA usually has a varying envelope, and to avoid distortion, advanced transmitting methods using different techniques, such as Envelope Elimination and Restoration (EER) or Polar transmitters [4]-[5], linear amplification with Nonlinear Components (LINC) [6]-[7], and sigma-delta based transmitters [8]-[9]-[10]. As a result; the envelope-varying signal is converted to a signal with a constant envelope. Consequently, it is possible to use highly efficient saturated linear amplifiers or switching-mode power amplifiers (SMPAs) such as classes D, E or F [11]-[12]-[13].

Digital transmitter architecture changes the signal to a bi-level constant envelope signal by using an oversampled sigma-delta modulator. This digital bi-level signal is ideal for use in conjunction with SMPAs. Therefore, digital transmitters not only satisfy the demand for reprogrammable, reconfigurable, multi-band, multi-standard transmitters for SDR, but also allow for the application of a sigma-delta modulation technique and, consequently, the use of power efficient SMPAs, while ensuring good linearity of the system.

Section II proposes ΣΔ-based digital RF transmitter architecture implementation at gigahertz frequency range, which is suitable for multiband multi-standard wireless communication applications. LP ΣΔMs are employed in the design which reduces the processing speed requirements. Section III introduces the design of the LP ΣΔM. Section IV introduces a complete design of multiband class-E PA. Finally, Section V is the conclusion.

2. The Proposed LP ΣΔM RF Based Transmitter Topology:

In band pass (BP) ΣΔMs, the output pulse width modulation (PWM) signal falls around a nonzero carrier frequency f_c, and the input signal is sampled at a frequency equal to at least four times the carrier frequency. In this way, the ΣΔ processor has to work at four times the desired carrier frequency. With today's digital technology, it is still very challenging to design an RF BP ΣΔM that works at gigahertz frequencies.

The major difference between this design and its BP ΣΔ is the use of the sigma delta modulator before up-converting the signal (in the baseband). This makes the required clock of the modulator equals to the sampling rate of the oversampled digital input which will be in the megahertz range (depends on the input signal bandwidth and the required oversampling ratio (OSR)).

In the proposed digital RF ΣΔ-based transmitter, a third order, single loop, switched capacitor architecture with a 1-bit quantizer is used to generate a bi- level signal, which is up converted to the desired/carrier frequency using a high speed multiplexer, using the pulse width modulated signal and its inversion. Finally a multi-band switching-mode PA with selected active power cell is used to amplify the bi-level RF signal at the output of the multiplexer. Before sending the signal over the antenna, a BP filter is used to suppress all the out-of-band distortions and to recover the amplitude and phase modulation of the analog RF signal.

Therefore, a reconfigurable multi-standard transmitter is achieved by only changing the clock frequency of the multiplexer and the carrier frequency so the signal standard can

be modified without any hardware modification. In order to ensure high efficiency, Class E PA is used.

3.The Proposed LP ΣΔM Topology:

Sigma-Delta modulators are the standard for analog to digital conversion (ADC) nowadays. It can achieve high signal to noise (SNR) ratio through the oversampling and noise shaping. It shapes the noise and pushes it out of the band of interest. Thus, low-power and high resolution of Sigma-Delta ADC can be achieved.

The resolution of the sigma-delta ADC can be increased by balancing three design aspects. They are the over-sampling ratio, order of the sigma-delta modulator and quantizer resolution. By using a higher order modulator, the signal to quantization noise ratio (SQNR) can be increased. The effect of noise shaping is clear from the following equation where L stands for the order of the filter [14],

$$\mathrm{SQNR} = 6.02N + 10(2L+1)\log(OSR) + 1.76\mathrm{dB} \quad (1)$$

Doubling the sampling frequency distributes this quantization noise over a wider frequency band than the signal bandwidth and, therefore, decreases the amount of noise in the signal band.

The quantizer transforms the amplitude modulated signal to a pulse-shaped bi-level signal and, at the same time, adds considerable quantization noise to the signal. The feedback loop shapes the noise outside the signal band, which further decreases the in-band quantization noise.

Further improvements in resolution can be obtained by using higher orders of noise shaping by using an L^{th} order modulator. Higher order modulators will lead to instability of the circuit and hence a feedback path is introduced to keep the system stable.

In the proposed transmitter design, a third order ΣΔM with CIFB (Cascade of Integrators Feedback) is employed as shown figure (2), taking into account the stability and SNR performance. Figure (3) shows the schematic of the 3rd order switched capacitor LP ΣΔM.

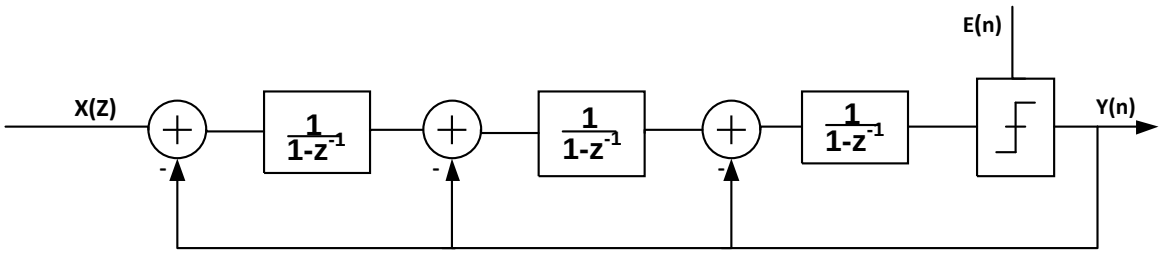

Figure (2): *Third-order LP ΣΔM block diagram*

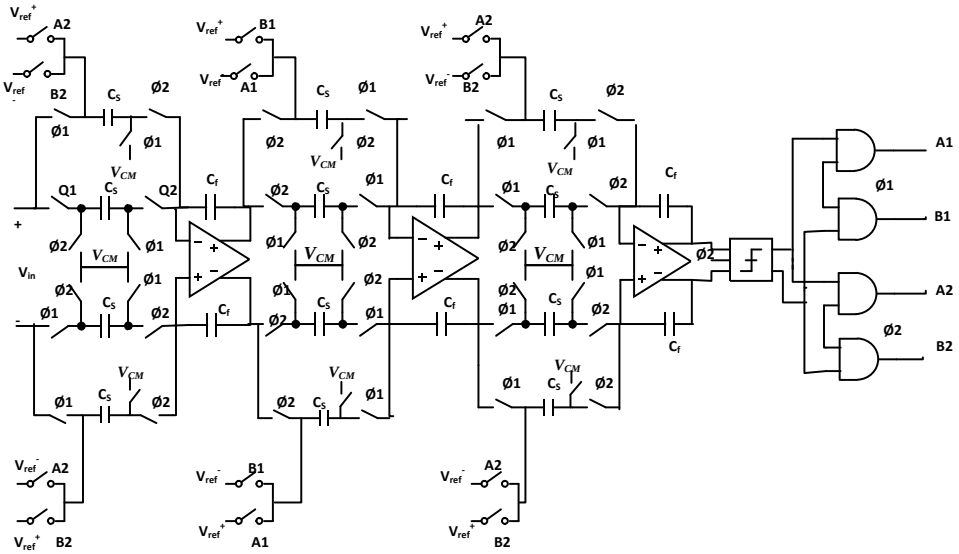

Figure (3): *The 3rd order switched capacitor LP ΣΔ modulator*

The switched capacitor clocks must be non-overlapping. The sampling capacitors CS and the feedback capacitors CF were chosen to provide the desired integrator gain. The switches were implemented as MOS transmission gates, which comprise the parallel connection of an NMOS and a PMOS switch to reduce the dependency of the on-resistance.

The proposed design has been implemented using switched-capacitors and simulated in TSMC 180nm CMOS technology. Figure (4) shows the modulator output in the time domain while Figure (5) shows the frequency domain representation of the output waveform. The noise shaping is very clear in figure (5).

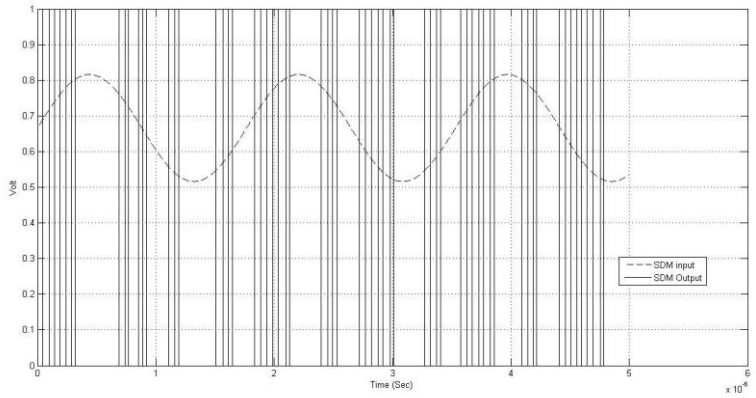

***Figure (4):** Modulator input and output waveforms*

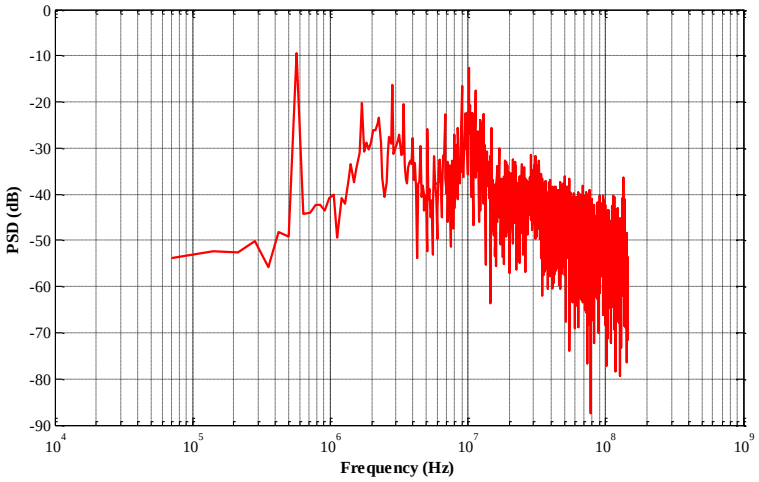

***Figure (5):** Power spectral density of the modulator output*

4. The Proposed Switching Mode Power Amplifier Design:

Using the low pass (LP) sigma delta modulator (ΣΔM) based architecture proposed in the previous section, the I/Q signals from the base band digital signal processing (DSP) are modulated and the modulated signal is transmitted to GHz carrier frequency by a digital approach. In this section, the idea of multi-band multi- standard power amplifier is demonstrated.

In wireless communication, portable devices are widely used, these devices are battery consuming and the battery life is very important. Since power amplifier is one of the most powers consuming element in the system, the efficiency of the power amplifier is one of the most important design considerations which secure longer the battery life

time and enable a smaller battery. The main concern in high power amplification is achieving high efficiency without degrading the quality of the output signal.

Generally, power amplifiers are classified according to mode of operation and the most general classification of power amplifiers are according to their linearity and efficiency. These two important criteria directly affect which class of amplifiers to be chosen for a design.

Switching mode power amplifiers use transistors as switches. Ideally, there is no power consumption at the transistor and the theoretical efficiency of the amplifier reaches to the level of 100%. Since using transistor as a switch means driving it into deep saturation, the analog interaction between the input and output signal will be lost that results in nonlinearity. Widely used switch mode amplifiers are Class-D, E and F.

Class-E power amplifier operates on the principle that no power should be consumed over the transistor. There is no overlap between the voltage and the current of the transistor. This results in zero power consumption over the transistor.

An equivalent circuit of an ideal single-ended Class-E power amplifier is shown in Figure (6) [15]. The circuit consists of a switching transistor (M1), a series-tuned output circuit (L_0 – C_0), shunt capacitors C_{DS} an RF choke inductance (L_{RFC}) and a load resistance ($R_{opt.}$). All these elements will be optimized to force the PA to work in class-E mode. The transistor will be used as a switching element.

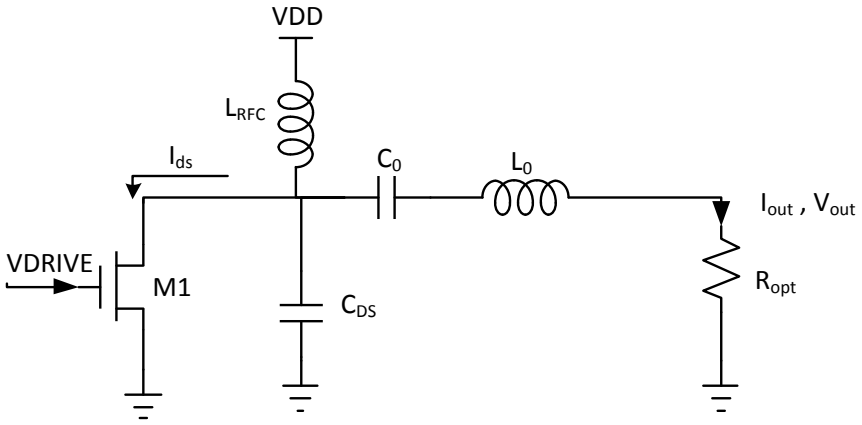

Figure (6): *Equivalent circuit of an ideal single ended class E power amplifier*

The class-E topology has the operation principle as explained when the transistor is `ON', the total current *Itot* flows through the transistor. At that time, the voltage over the transistor (also over the capacitor) is zero, so no current flows through the capacitor.

When the transistor is `OFF', no current flows through the transistor and the total current I_{tot} flows through the capacitor. This voltage-current characteristics result in no power dissipation over the transistor. The resonant circuit of the series-tuned output circuit provides fundamental current owing through the load. Since the reactance of the resonant circuit is very high at the harmonic frequencies, no harmonic power dissipation occurs. All these properties provide Class-E topology to achieve 100% theoretical efficiency.

The proposed PA with selective operation of the power transistor cells is a two-stage differential amplifier with a cascode structure in the power stage as shown in figure (7). The PA also uses a wideband driver stage. To reduce the transistor component count, the common source (CS) amplifier of each differential cascode power stage is shared by the two common gate (CG) amplifiers.

The CG amplifiers CG (LB) and CG (LB) are assigned for RF OUT1 path (the 1.8 GHz GSM, 1.9 GHz LTE), and CG (HB) and CG (HB) for RF OUT2 path (the 2.1 GHz UMTS, 2.4 GHz WI-FI and 2.6 GHz LTE). When the appropriate bias voltage is applied to the gate and the drain of both CG (LB) and CG (LB) and not to those of CG (HB) and CG (HB), the RF OUT1 path is turned on and the RF OUT2 path is turned off, and vice versa.

To satisfy broadband characteristic operation from 1.8GHz to 2.6 GHz, three stages inverter type class D power amplifier with a feedback resistor between the input and output part of the amplifier is considered for solving the bias stability problem and to enhance the voltage gain.

In order to protect against limitations of low breakdown voltage with a single transistor as the swing from input voltage will cause large stress on the gate oxide, a cascade structure is employed. Cascode structure allows the top transistor to have its gate oxide stress reduced by providing it a constant gate biasing. Also, a differential topology helps in suppressing spurious injection from other blocks because of the common-mode rejection; it eliminates even-order harmonics. This means, there is no need for a second harmonic resonator as compared to single-ended design and it also enhances output voltage swing. The PA has 3.3 V V_{DD} and 0.8 V V_{GS} for the power stage and 2.5 V V_{DA} for the driver stage. The cascade common gate bias is 2.5 V for both Vbias_LB and Vbias_HB.

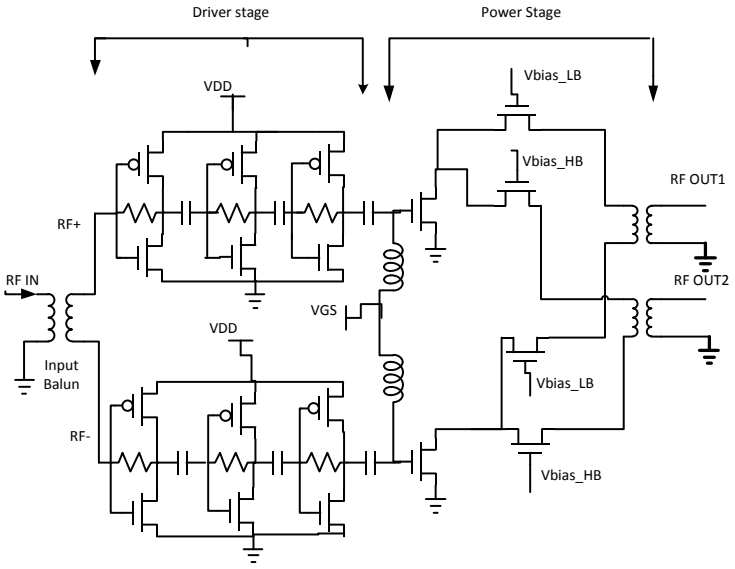

Figure (7): *Schematic of the designed class-E multi-band PA*

Figure (8) shows the time domain representation of the drain current versus the drain voltage. The simulation results of the output power and the power added efficiency (PAE) at RF OUT1 port for 1.8/1.9GHz signals and RF OUT2 port for 2.1/2.4/2.6 GHz signal, the maximum output power (Pout) is 27.7/27.5/27.6/27/26.7dBm and the power added efficiency (PAE) is 62/58.7/60/52/47% in continuous wave (CW) mode for the 1.8/1.9/2.1/2.4/2.6GHz, respectively figure (9) and figure (10).

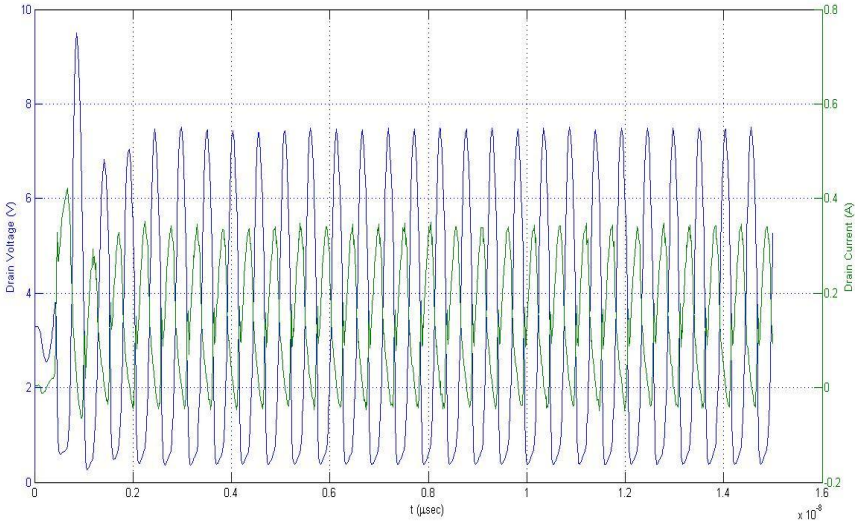

Figure (8): *Simulated time domain of the drain voltage and the drain current at 1.9 GHz*

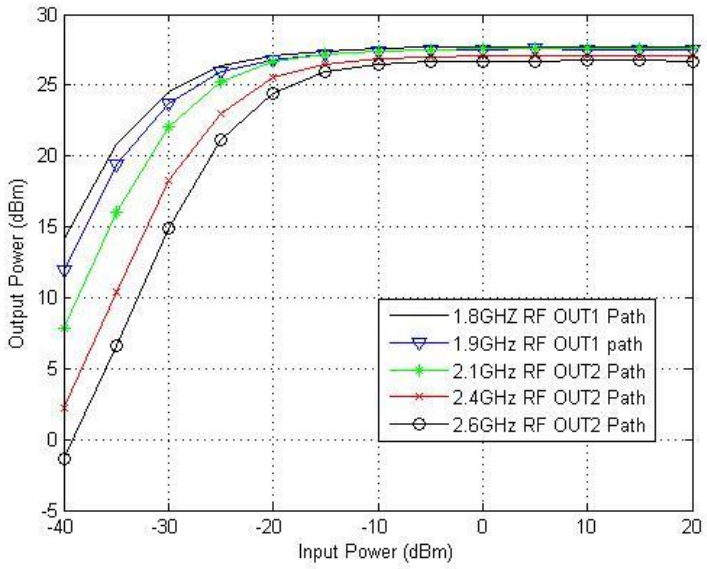

Figure (9): *Simulated output Power versus input power at 1.8/1.9/2.1/2.4/2.6 GHz*

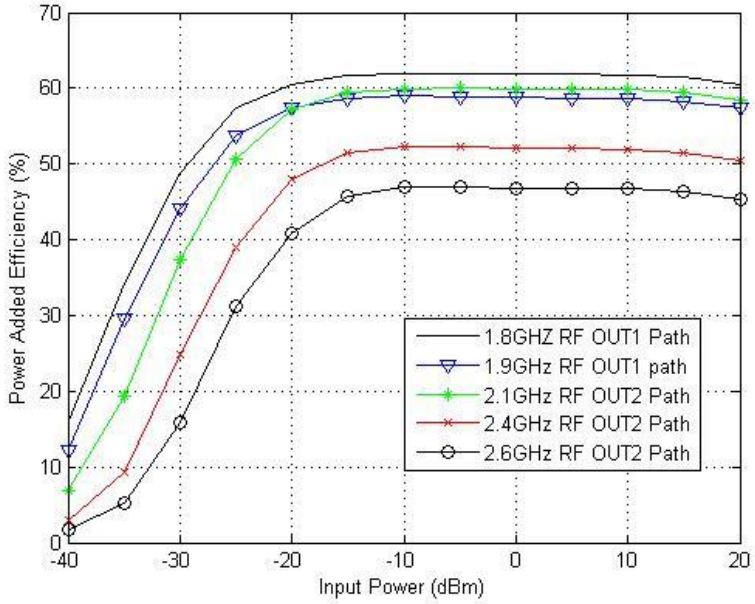

Figure (10): *Simulated PAE versus input power at 1.8/1.9/2.1/2.4/2.6 GHz*

The PAE for RF OUT2 is lower than that of RF OUT1 due to the parasitic capacitance of C_{gs}. Each CG has the same size of transistor in both the LB and HB. As the frequency increases, parasitic capacitance of C_{gs} makes more influence to the PA and this leads to

the degradation of the PAE.

From the simulation results, it is noticed that designed multiband/wideband PA can cover many frequency bands while maintaining high efficiency.

In figure (11) the complete schematic of the proposed third order LP ΣΔ modulator driving a switched mode class E PA is shown.

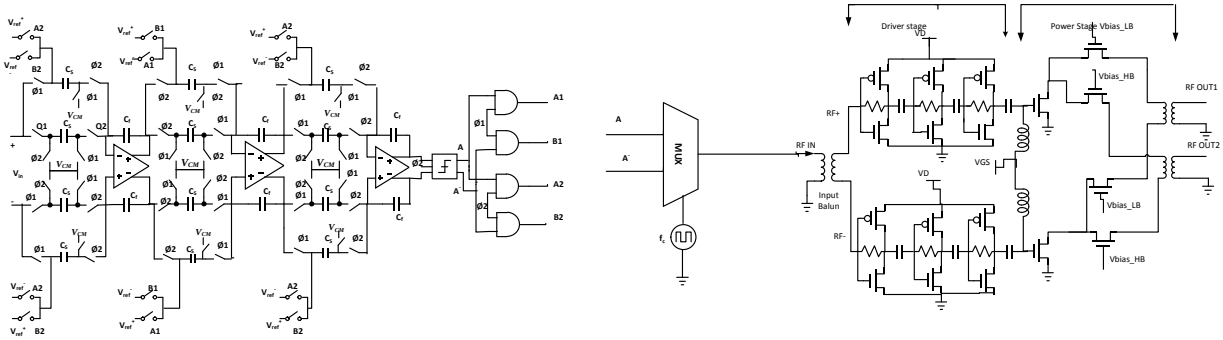

Figure (11): *Complete schematic of LP ΣΔ transmitter driving a switching mode class E PA*

Figure (12) shows the simulation result of the time domain representation of the drain current versus the drain voltage with a clock frequency of the multiplexer 2.4GHz.

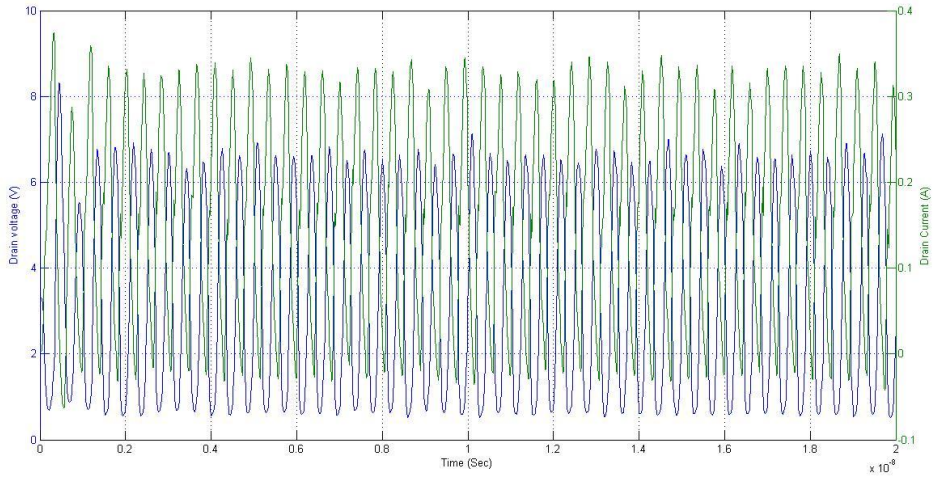

Figure (12): *Simulated drain voltage and drain current of the complete schematic at 2.4 GHz*

5. CONCLUSION:

This paper presents a sigma delta modulator (ΣΔM) based transmitter that is suitable for digital multi-standard wireless applications especially for software defined radio (SDR) systems. In the proposed design, a third order low-pass ΣΔM is implemented to produce a high frequency digital-like signals that is used to drive a high efficient class-E switching mode power amplifier.

The target technology for fabrication is TSMC180nm CMOS process. The proposed design is tested for different standards such as GSM, UMTS, Wi-Fi and LTE. The saturated output power (Pout) is 27.7/27.5/27.6/27/26.7dBm and the power added efficiency (PAE) is 62/58.7/60/52/47% in continuous wave (CW) mode for the 1.8/1.9/2.1/2.4/2.6 GHz, respectively.

From the results, it is clear that the designed multiband/wideband PA can cover many frequency bands while maintaining high efficiency which make it suitable for multiband wireless communication systems.

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Nomenclatures:

L … Order of the filter
$\emptyset_1, \emptyset_2$ Non - overlapping clocks
V_{ref} Reference voltage
C_s, C_f Sampling capacitor and feedback capacitor respectively