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Integrated Chip Current Mode DC-DC Buck Converter for Wireless Power Receiver

By

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Abstract:

In this paper, we propose integrated chip DC-DC buck converter for wireless power receiver. The control of DC-DC buck converter is designed by current-mode technique. The DC-DC converter is an essential power management circuit that adjusts the output voltage based on portable electronic device applications. In addition, it reduces the energy loss due to thermal degradation and noise generated at power transmission. Therefore, DC-DC converter that operates at high efficiency is a major design constraint for wide input voltage variation. The proposed DC-DC converter is implemented and fabricated using 0.18μm BCD process. The DC-DC converter comprises of OTA, compensator, current sensing circuit, clock and ramp signal generator and a comparator. It is designed for 85% peak efficiency with a 1MHz switching frequency, 5.5V to 10V input voltage and 400mA maximum load current. The maximum accuracy for sensing current reaches 99%.

Keywords:

Wireless power transfer, DC-DC converter, current sensing circuit, operational transconductance amplifier, compensator, comparator and clock and ramp signal generator

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1. Introduction:

Recently, there has been an increasing interest in wireless power transfer due to the development of mobile devices, smart application devices, biomedical devices and electronic vehicles. The wireless power transmission (WPT) technologies can be divided into two methods, inductive coupling and magnetic resonance coupling.
WPT which is based on inductive coupling demonstrates high efficiency, however, they are limited to several tens of mm in power transfer range [2]. Meanwhile, the magnetic resonance coupling method using magnetic evanescent wave coupling was a potential breakthrough, for mid-range energy transfer [1], [3], [4].

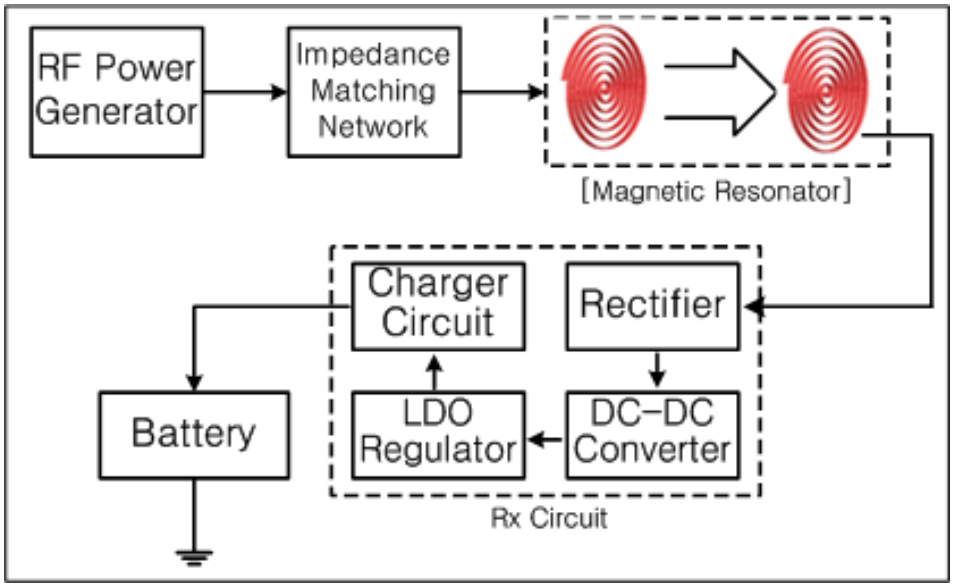

Figure (1): *Magnetic resonance wireless power transfer system block*

Figure (1) is a general block diagram of magnetic resonance WPT scheme. The integrated power receiver contains a rectifier, DC-DC converter, LDO regulator and battery charge control circuit for mobile applications. The important feature of WPT is high efficiency at large transmission distance. The variation in the impedance of the power receiving circuit, changes the efficiency of power transmission system randomly. The impedance transformations are mainly due to voltage changes and the change in distance between the transmitter and receiver. Therefore, DC-DC converter is able to improve efficiency by regulate load voltage. In paper [5], experiment shows that efficiency of power transmission is increased by DC-DC converter. In addition, in WPT system, the process of converting the voltage which is transferred to a particular application is very important.
In this paper, we have designed a current mode DC-DC buck converter that is included

in the Rx circuit of WPT system. The converter controller is using pulse width modulation (PWM) method since WPT uses a large load currents.

2. Current mode DC-DC buck converter:

A. DC-DC converter with inductor

DC-DC converter with inductor step-up or step-down the input voltage based on application [6], [7], [8], [9]. In general, method for designing current mode controller of DC-DC converter with inductor can be divided into two. The first method is pulse frequency modulation (PFM). PFM controller have simple structure since it is constitute of a comparator and shows high efficiency at low load currents. However, it is very difficult to filter the switching noise due to variation in switching frequency characteristic. The second method is pulse width modulation (PWM) that have constant switching frequency. This method is used in sensitive systems to reduce noise. Therefore, in general, a system that uses a large load current is using PWM control method [10].

B. Current mode DC-DC buck converter

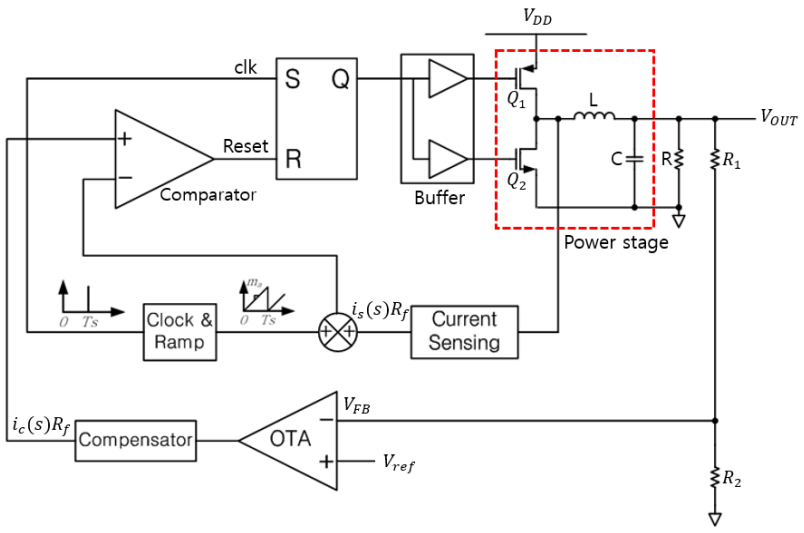

Figure (2): *Block diagram of current mode DC-DC buck converter*

Inductor type of DC-DC converter is a non-linear circuit that operates by switching. In such a circuit, it requires small signal model that is linearized in order to analyze the stability of the feedback loop. General voltage mode DC-DC buck converter is difficult to secure the gain and phase margin because this converter has two poles [11], [12].

The voltage mode DC-DC buck converter uses proportional integral derivative (PID) compensator which can compensate the gain and phase margin at the same time [12]. The current mode DC-DC buck converter has two poles such as the voltage mode DC-DC buck converter [13]. However, Second pole frequency of current mode DC-DC converter is far away from the first pole frequency. Thus second pole does not affect the stability of the entire converter [13], [14], then it has appropriate phase margin without phase lead network. Therefore, current mode DC-DC converter compensates only gain using proportional integration (PI) compensator.

The oscillation due to Disturbance is a drawback of the current mode that is well known. The current mode DC-DC converter control signal with the inductor current is sensitive to disturbance [13]. To prevent this oscillation due to disturbance, adding artificial ramp to the current sensing signal is essential.

Figure (2) represent a simplified block diagram of current mode DC-DC buck converter. The main function of the converter is to convert the voltage to a lower output voltage than the input voltage. This converter consist of power supply part and feedback control part. V_{DD} is the input voltage and V_{OUT} is the output voltage. R_1 and R_2 detect the output voltage and determines the value of output voltage of the operational transconductance amplifier (OTA). In Figure (2), the clock generates a short pulse wave having the determined pre-cycle, the output of the SR latch is determined by this pulse. A reset timing of the latch is controlled by a comparison of $i_c(S)R_f$ through the OTA output and $i_s(S)R_f$ through the inductor sensing current circuit. Flowing current in Q1 is equal to inductor current. This means that the signal of the current sensing circuit $i_s(S)R_f$ is same as inductor current. When Q_1 is set on, output voltage increases. If V_{ref} is not equal to the output voltage that is measured via (R_1, R_2), the control signal is changed by the OTA, so that it becomes to adjust the output voltage due to a reset timing of the latch is changed. In other words, the operation of the transistors (Q_1, Q_2) is controlled by the PWM signals generated by the latch and it bring to generate the desired output voltage through transistor On/Off operation [11], [12].

C. OTA and compensator circuit

For the design of compensator initially, the unit-gain frequency has to be define. If unit-gain frequency has decided, it is possible to determine the gain and amount of phase compensation. In general, unity-gain frequency is less than 1/10 of the converter switching frequency. If more than 1/10 of the converter switching frequency, a gain of compensator is to be too large, then switching noise is amplified by the compensation will affect the internal converter [13], [14]. After determining the unit-gain frequency, we decide pole and zero frequency and gain of unit-gain frequency. In this case, median of zero and pole frequency will be determined to match the unit-gain frequency to prevent the decrease in phase margin.

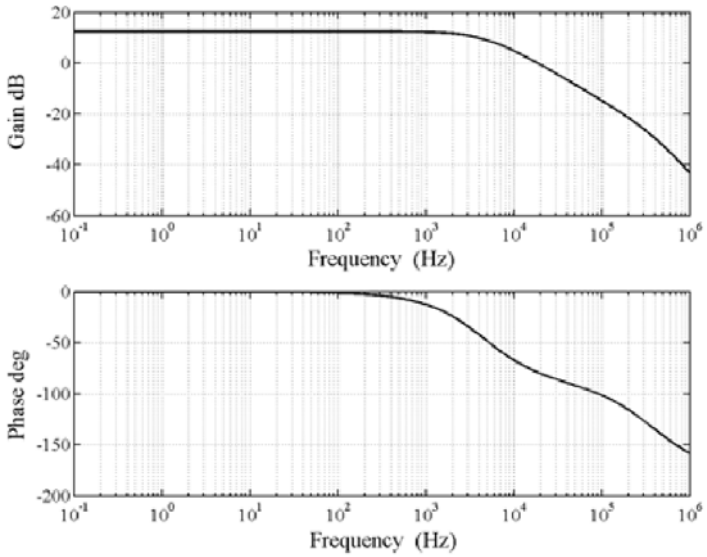

Figure (3): *Frequency characteristics of buck converter without compensation*

Figure (3) represent the frequency characteristics of uncompensated current mode DC-DC converter. it can be approximated to the first order model of a single pole. The current mode DC-DC converter without compensation has a sufficient phase margin. But DC gain is very low less than 20dB, so it should be compensated by the proportional integration (PI) compensator.

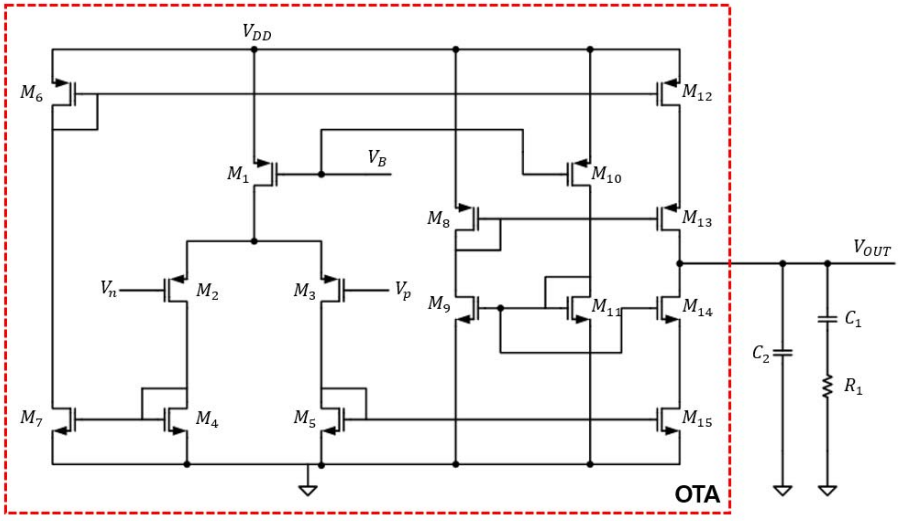

Figure (4): *OTA circuit and PI compensator using OTA*

Figure (4) shows OTA circuit diagram and proposed PI compensator. In proposed PI compensator, pole and zero frequency are given by equation (1) and (2).

$$f_z = \frac{1}{2\pi R_1 C_1} \tag{1}$$

$$f_p = \frac{C_1 + C_2}{2\pi R_1 C_1 C_2} \approx \frac{1}{2\pi R_1 C_2} \qquad \text{where } C_2 \ll C_2 \tag{2}$$

The gain of compensator in unit gain frequency is given by equation (3)

$$A_v = g_m R_1 \tag{3}$$

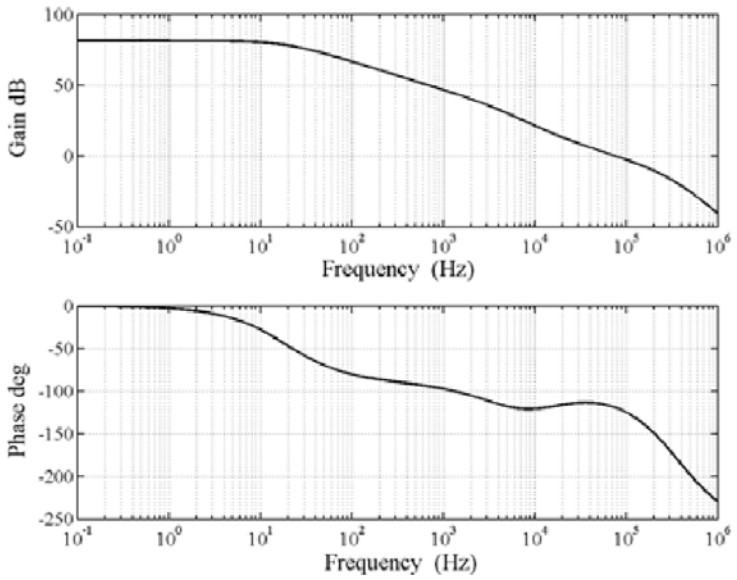

Figure (5): *Frequency characteristics of compensated buck converter*

Figure (5) represent frequency characteristics of compensated current mode DC-DC buck converter. The gain and phase characteristics were compensated sufficient DC gain and phase margin through the PI compensators.

D. Current sensing circuit

Figure (6) shows the proposed current sensing circuit. A pair of cascade common gate amplifiers achieve high loop gain. The bulks of M_{P9} and M_{P10} are connected to node C and D. Thus it can provide two additional inputs for the cascade common gate amplifier to improve loop gain and transient response. The cascade current mirror composed of M_{N2}-M_{N5} increases the output impedance of the common gate amplifier and reduce the channel length modulation effect. A small input offset voltage between node A and B according to the negative feedback loop of M_{P4} causes the sensing current IS to

decrease. As a result, V_B is increased due to increase in gate voltage of M_{P4} in at saturation region. Therefore, high loop gain and small offset voltage provide high sensing accuracy since the negative feedback forces V_B to change in the same direction as V_A

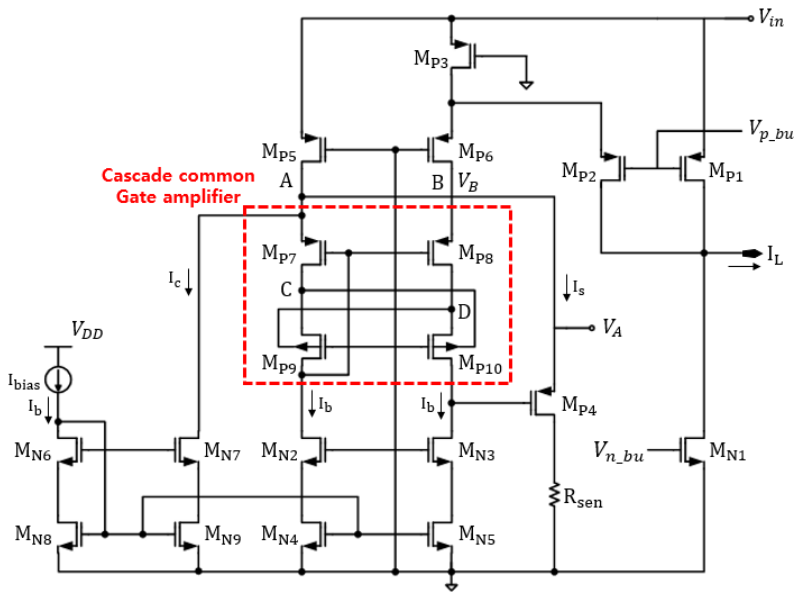

Figure (6): *Current sensing circuit*

E. Clock and ramp signal generator

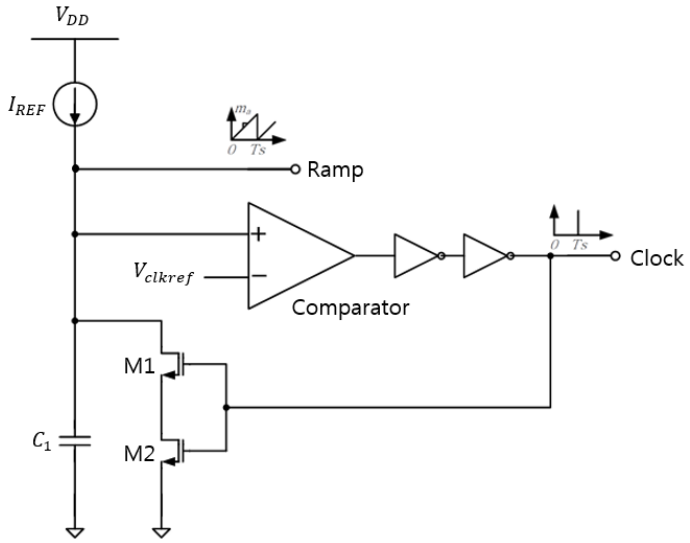

Figure (7): *Clock and Ramp signal generator*

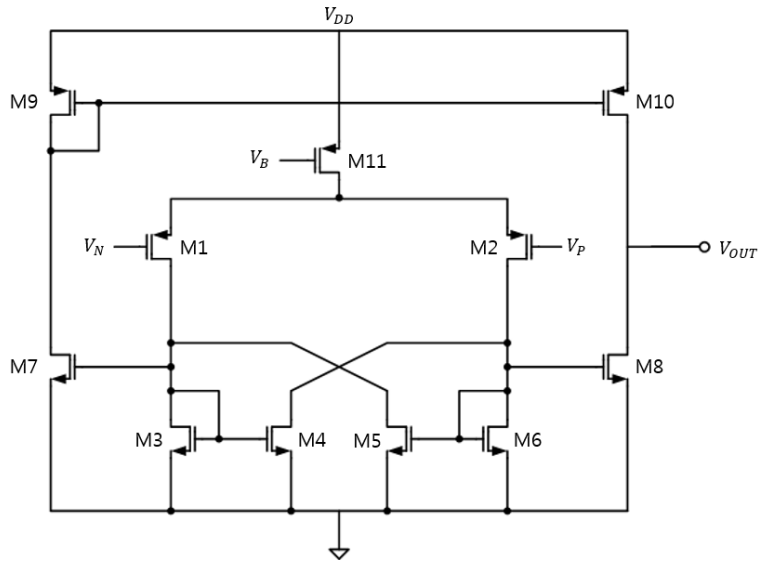

Figure (8): *Hysteresis comparator*

The schematic of clock and ramp signal generator is shown in the figure (7). This circuit generate the clock and ramp signal for PWM signal control and stability of the current sensing. The schematic circuit of comparator is shown in fig. 8. When the capacitor C1 is charged by the current source, the voltage of ramp node increases according to the following equation (4).

$$Ramp = \frac{I_{REF}}{C_1} \cdot t \tag{4}$$

When the ramp voltage increase until V_{CLEREF}, M1 and M2 is turn on, then C_1 is discharged. As a result, lamp node voltage to be reduce. When C_1 is discharged, so much current flows in to the capacitor momently. It is able to lead to destruction of the transistor. Therefore, M1 and M2 transistor was placed in series to prevent destruction of transistor. While repeating the above process, signal generator produces the desired signal.

3. Result:

The proposed current mode DC-DC buck converter for wireless power receiver was implemented by using 0.18μm BCD process. The maximum accuracy for sensing current reaches 99%. Figure (9) represent a waveform that is output voltage according to Instantaneous changes in load current. The load current is changed from 400mA to 100mA and 400mA to 100mA. The pulse load response of the DC-DC converter for 100mA-400mA change is depicted on figure (9).

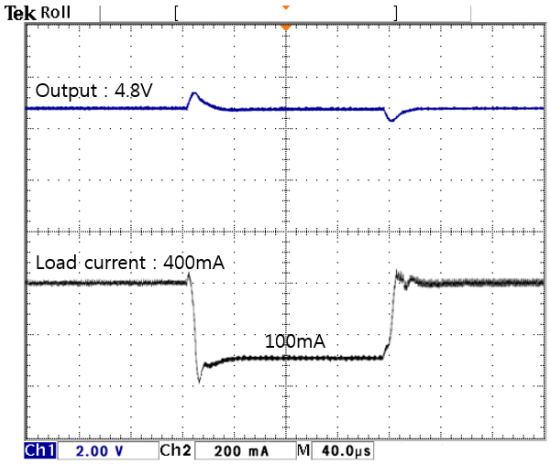

Figure (9): *Output voltage variation by load current changing*

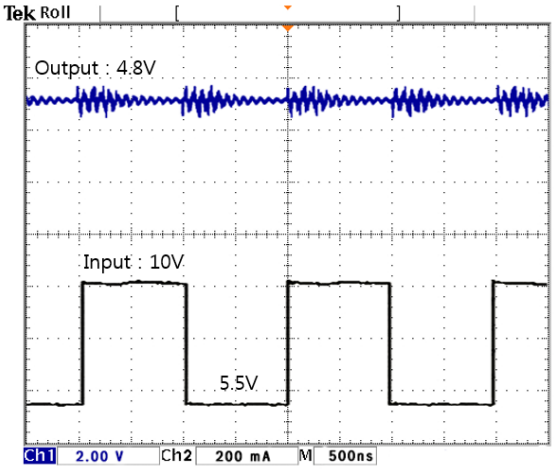

Figure (10): *Wave form of DC-DC converter*

Figure (10) shows the transient wave form of fabricated DC-DC converter for pulse input of 5.5V to 10V at 1MHz and 400mA output current. The overall maximum efficiency is about 85%. Figure (11) shows die microphotograph of the fabricated chip.

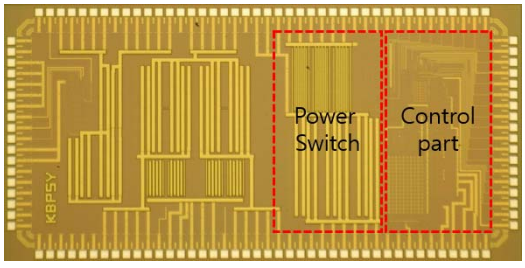

Figure (11): *Die microphotograph of the fabricated chip*

4. Conclusion:

In this paper, we proposed current mode DC-DC buck converter for magnetic resonance wireless power transfer. It was implemented by using 0.18μm BCD process. DC-DC converter has 1MHz operating frequency and 400mA maximum load current performance. The maximum accuracy for sensing current reaches 99%. The overall maximum efficiency of the fabricated chips is about 85%

References:

[1] A. Kurs, A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, and M. Solja˘ci´c, *Wireless power transfer via strongly coupled magnetic resonances*, Science, vol. 317, no. 5834, pp. 83-86, July 2007.

[2] William C. Brown, *The History of Power Transmission by Radio Waves*, IEEE Trans, micro. theory tech,. vol. MTT-32, no.9, pp. 1230-1242, Sept. 1984.

[3] A. Karalis, J. D. Joannopoulos, and M. Solja˘ci´c, *Efficient wireless non-radiative mid-range energy transfer*, Ann.Phys., vol. 323, no. 1, pp. 34- 48, January 2008.

[4] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, 2nd ed. New York, NY: IEEE Press and John Wiley & Sons, 2011, no. 978-0-470-90538-8.

[5] Yusuke Moriwaki, Takahiro Imura and YoichiHori, *Basic study on reduction of reflected power using DC/DC converters in wireless power transfer system via magnetic resonant coupling*, INTELEC, vol.33, pp.230-234, Oct.2011.

[6] C. Y. Leung, P. K. T. Mok, K. N. Leung, and M. Chan, *An integrated CMOS current-sensing circuit for low-voltage current-mode buck regulator*, IEEE Trans. Circuits Syst. II, vol. 52, no. 7, pp. 394394, Jul. 2005.

[7] H. P. Forghani-zadeh, and G. A. Rincon-Mora, *An accurate, continuous, and lossless self-learning CMOS current-sensing scheme for inductor based DC-DC converters*, IEEE J. of Solid-State Circuits, vol. 42, pp.665- 679, Mar. 2007.

[8] J. Chen, J. Su, H. Lin, C. Chang, Y. Lee, T. Chen, H.Wang, K. Chang, and P. Lin, *Integrated current sensing circuits suitable for step-down DC-DC converters*, Electron. Lett., pp. 200-201, Feb. 2004.

[9] H. Deng, X. Duan, N. Sun, Y. Ma, A. Q. Huan, and D. Chen, *Monolithically integrated boost converter based on 0.5-μm CMOS process*, IEEE Trans. on Power Electronics, vol. 20, pp.628-638, May 2005.

[10] Jeongjin Roh, Donghun Heo, Kitae Kim, Hyunseok Nam, Youngkil Choi, Hyungdong Rho, *A 900nA quiescent current Buck converter with on-chip compensator*, ITC-CSCC 2006, PP.413-416, July 2006.

[11] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Boston, MA: Kluwer, 2000.

[12] I. Pressman, *Switching Power Supply Design*, 2nd ed. New York: Mc- Graw-Hill, 1998.

[13] P. T. Krein, *Elements of Power Electronics*, McGraw-Hill, 1998.

[14] M. Brown, *Practical Switching Power Supply Design*, San Diego, CA: Academic, 1990.