Military Technical College
Kobry El-Kobbah,
Cairo, Egypt

10th International Conference
on Electrical Engineering
ICEENG 2016

A Low-Power Low-Noise Neural recording Bioamplifier

By

Tamer Farouk
Department of electronic engineering
Military technical college
Cairo, Egypt
Tamerfarouk76@yahoo.com

Mohamed Elkhatib
Department of electronic engineering
Military technical college
Cairo, Egypt
elkhatib.m@gmail.com

Mohamed Dessouky
ECE department
Ain shams university
Cairo, Egypt
mohamed.dessouky@eng.asu.edu.eg

Abstract:

This paper presents a low-voltage low-power low-noise amplifier suitable for neural recording applications. The amplifier is able to operate under a 1V supply by alleviating the tradeoff between the noise and the voltage headroom. The amplifier is based on a gm-cell, such that its effective transconductance is not a function of the bias current. As a result the noise contribution of the output transistors can be decreased without increasing the bias current. This bioamplifier rejects DC offset voltage using active low frequency suppression instead of AC coupling capacitors to achieve reduced-size and higher input impedance. The bioamplifier is designed for neural recording of action potentials and simulated in a 130 nm CMOS process. The amplifier consumes 5.2 µW from 1V supply voltage. The input referred noise is 4.7 µVrms¬¬. The amplifier has a Bandwidth (BW) from 110 Hz to 9.7 kHz.

Keywords:

Biopotential amplifier, low noise, low power circuit design, neural amplifier

1. Introduction:

Biopotential amplifiers are used to sense very weak signals using an electrode. The performance of the system used in neural recording depends on the performance of the amplifier as it is the first stage of the system. The bio potential amplifier rejects the DC offset voltage developed at the electrode body interface. The signal amplitude of the extracellular action potential is up to 500 μV, with energy lays in the 100Hzto7kHz band [1], so with this weak input signal the amplifier must provide low input referred noise to maintain a reasonable dynamic range. The biopotential amplifier should achieve a low power low voltage operation to minimize heat dissipation which could damage the surrounding tissues, avoid frequent battery replacement and reduce the size of the power source.

One of the early techniques used for designing biopotential amplifiers is the circuit reported in [1] as shown in Fig. 1. This technique includes the usage of capacitive coupling to reject DC offset, using $M_a - M_d$ as a pseudo-resistors with capacitive feedback around the operational transconductance amplifier (OTA) to achieve a low cut-off frequency of the high-pass filter. This approach has disadvantages that it may degrade the input-referred noise, lower the input impedance of the amplifier, subject to mismatch in passive input devices, and it requires very large integrated capacitors that dominate the amplifier area in order to achieve satisfactory gains.

Another technique used to build bioamplifier is the one reported in [2] as shown in Fig. 2. This technique uses the active low frequency suppression scheme to reject DC offset. An active integrator located in the feedback path of a low-noise amplifier employed for placing a highpass cutoff frequency within the transfer function. This configuration rejects unwanted low-frequency contents without the need for large input AC coupling capacitors. Therefore, the bioamplifier high-input impedance and small size are preserved.

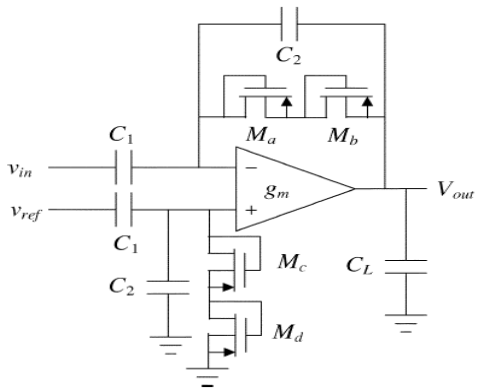

***Figure (1):** Schematic of neural amplifier [1] with ac coupling capacitors*

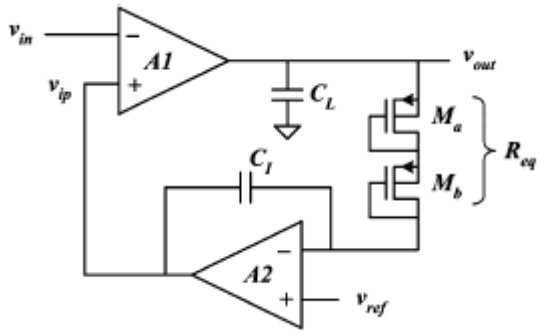

***Figure (2):** Schematic of neural amplifier with active low frequency suppression*

These reported techniques use a one-stage current mirror operational transconductance amplifier (OTA) to achieve a low noise operation by making the noise contribution of the input transistors more dominant. In fact, the aspect ratio of the output transistors should be made much smaller than that of the input transistors. However, for a certain bias current decreasing the aspect ratio of the output transistors results in increasing the overdrive voltage which decreases the available headroom. Thus, a tradeoff between the noise and the voltage headroom is required at the output. Also, decreasing the noise contribution of the output transistors can be achieved by increasing the transconductance of the input transistors but the transconductance is limited by the given bias current. To overcome this problem, the proposed OTA contains a gm-cell with an overall transconductance Gm independent of the bias current as in [3].

In this paper, a low-voltage low-power low-noise OTA is proposed as a further enhancement of that presented in [3]. Section (2) introduces the proposed OTA. Section (3) shows the simulation results of the whole biopotential amplifier with the proposed OTA. Finally, section (4) concludes the paper.

2. The proposed OTA

The proposed OTA is based on the flipped voltage follower (FVF) [4]. As shown in Fig.3, the FVF is used to build a gm-cell whose effective transconductance (Gm) is not a function of the bias current.
The current of M1, M2 is held constant equal to I_B.

$$V_{s1} = V_{in+} - V_{GS1} \quad , \quad V_{s2} = V_{in-} - V_{GS2} \tag{1}$$

$$V_{s1} - V_{s2} = V_{in+} - V_{in-} = v_{ind} \quad , \quad I_R = v_{ind}/R \tag{2}$$

The negative feedback adjusts I_3, I_4 as follows

$$I_3 = I_B - I_R \quad , \quad I_4 = I_B + I_R \tag{3}$$

$$i_{od} = I_4 - I_3 = 2I_R \tag{4}$$

$$G_m = i_{od}/v_{ind} = 2/R \tag{5}$$

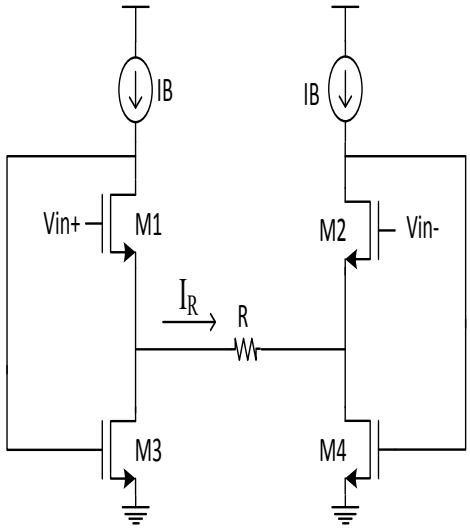

***Figure (3):** A gm-cell based on FVF [4]*

Figure 4 shows the proposed OTA where the output current of the gm-cell is converted to a single ended output by M5-M8. The level shifter is a common drain voltage follower as shown in Fig. 5, it consumes 0.1 μA. It is used to ensure that the input transistors operate in the saturation mode.

The amplifier A2 used in the integrator is a miller OTA with current consumption 3uA, the bias current of the input transistors of A2 is 1uA which is double the current in the main OTA A1. This will result in making the noise of the main OTA A1 to be dominant and to minimize the noise of the integrator.

The input referred noise can be given by

$$\overline{V_{n,in}^2} = 4KT\left[\frac{4}{3g_{m1}} + R + \frac{2}{3}\frac{4g_{m3}+2g_{m7}}{G_m^2} + \frac{4}{3}g_{m9}\left(\frac{1}{g_{m1}}+\frac{R}{2}\right)^2\right] \tag{6}$$

$$\overline{V_{n,in}^2} \approx \frac{16KT}{3g_{m1}}\left[1+\frac{g_{m9}}{g_{m1}}\right] + \frac{16KT}{3G_m}\left[\frac{2g_{m3}+g_{m7}}{G_m}\right] \tag{7}$$

The noise contribution from the transistors M3-M8 can be extremely reduced by increasing Gm (decreasing R). There is no need to decrease the aspect ratio of the output transistors, so the tradeoff between the noise and the voltage headroom is eliminated. The overdrive voltage of the output transistors is kept under 50mV, which

allows a rail to rail operation. The noise contribution of the level shifter transistors can be neglected because its input referred noise is proportional to g_{mL}/G_m where g_{mL} is the transconductance of the level shifter transistor. The only two transistors that is needed to decrease their aspect ratios are M9 and M10 because their input referred noise is proportional to g_{m9}/g_{m1}, but their overdrive voltage will not affect the available headroom at the output.

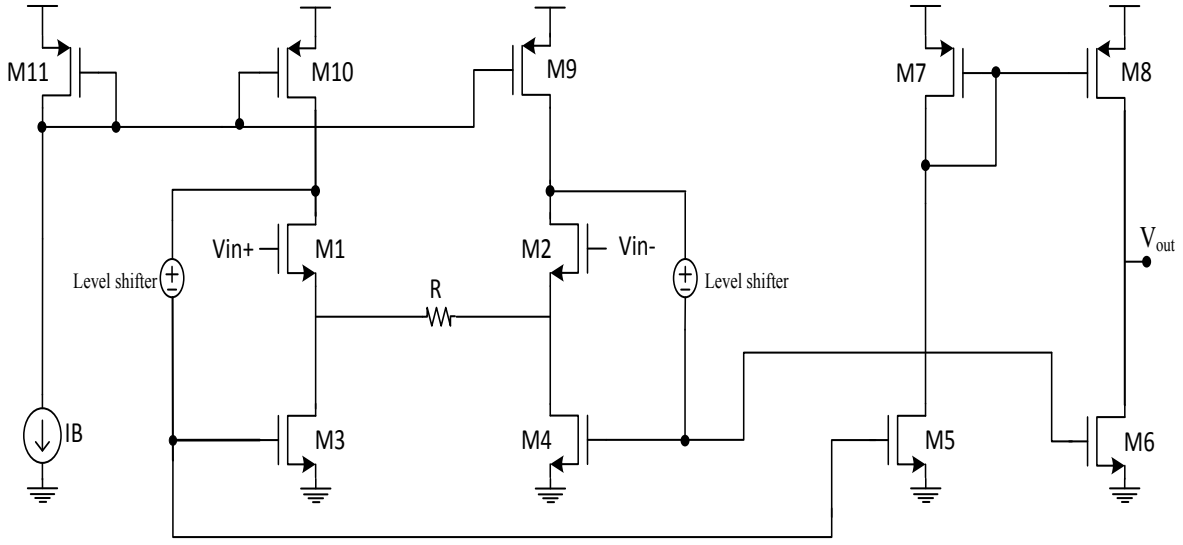

Figure (4): *The proposed OTA*

3. Simulation results of the biopotential amplifier

The amplifier shown in Fig. 2 using the proposed OTA shown in Fig. 4 as A1 is designed and simulated in a 130 nm CMOS process. The mid-band gain $A_m = A_{o1}$ is 52dB. The high pass cutoff frequency $f_{hp} = A_{o1}/2\pi R_{eq} C_2$ is 110 Hz. The low pass cutoff frequency is defined by the A1 dominant pole $f_{lp} = 1/2\pi R_{out} C_L$ is 9.7 kHz. Where R_{eq} is the equivalent resistance of the pseudo-resistors, R_{out} is the output resistance of A1. Fig. 6 shows the frequency response of the amplifier.

Table (1) shows the dc operating points and the dimensions of the transistors used in the OTA. The total current consumption is 5.2µA from a 1V supply, which means the power consumption is 5.2µW.

The noise efficiency factor (NEF) is used as a figure of merit to compare the noise and

power performance with other amplifiers [5].

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi V_T 4KT(BW)}} \quad (8)$$

Where $V_{ni,rms}$ is the input referred rms noise voltage, I_{tot} is the total amplifier supply current, and BW is the amplifier bandwidth. The proposed OTA achieves NEF of 4.27 which is a reasonable NEF for a small area amplifier as shown in Table (2).

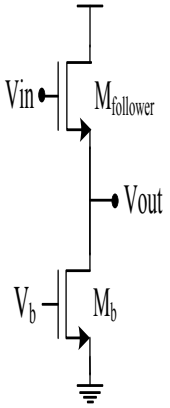

Figure (5): *Level shifter*

Table (1): *Devices geometry and DC bias current for OTA*

Devices	W/L(μm)	I_D(μA)
M1,M2	300/1.5	0.5
M3, M4, M5, M6	5/0.31	0.5
M7, M8	2/0.31	0.5
M9, M10, M11	2/40	0.5
M_b, $M_{follower}$	1/8	0.1

Fig. 7 shows the simulated input-referred voltage noise spectrum. The thermal noise level is 38 nV/√Hz and the noise corner occurs around a few hundred Hz. Integration of the output voltage noise from 0.1 Hz to 100 kHz then dividing the result over the amplifier mid-band gain yields an input referred noise voltage of 4.7 μVrms.

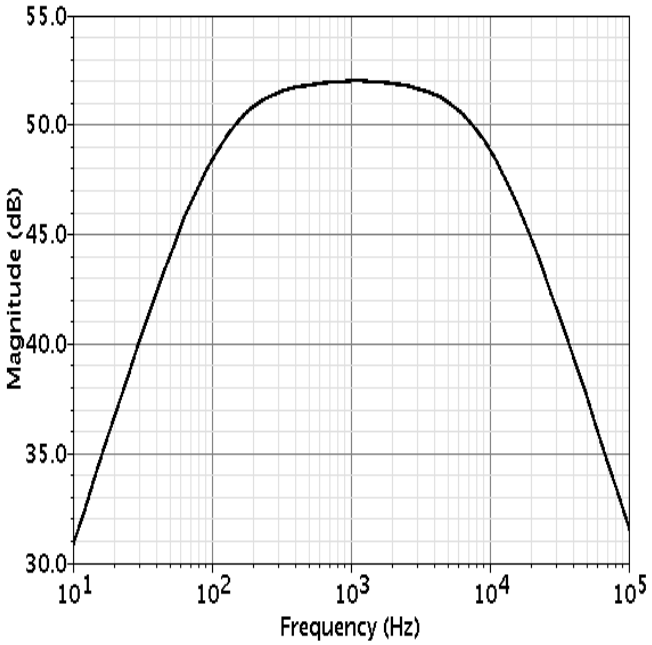

Figure (6): *The frequency response of the amplifier.*

The proposed amplifier achieves a low input referred voltage noise with a low power consumption and can operate under 1V power supply with rail to rail output swing, it achieves the a reasonable NEF with occupying small area due to decreasing the total capacitance used in the design.

Table (2): *Performance comparison of biopotential amplifiers*

		BW (Hz)	Gain (dB)	NEF	$V_{in,rms}$ (μV)	Supply (V)	Power (μW)	Tech. (μm)
Harrison 2003	[1]	0.025-7.2k	39.5	4	2.2	5	80	1.5
Wu 2006	[3]	0.003-245	40.2	3.8	2.7	1	2.3	0.35
Wattanapanitch 2007	[6]	45-5.3k	40.9	2.7	3.1	2.8	7.56	0.5
Gosselin 2007	[2]	105-9.2kHz	52	4.9	5.6	1.8	8.6	0.18
Rezaee 2011	[7]	300-10k	57.5	3	2.4	1.8	20.8	0.18
Majidzadeh 2011	[8]	10-7.2k	39.4	3.35	3.5	1.8	7.92	0.18
Qian 2011	[9]	0.36-1.3k	39.4	3.09	3.07	2.8	2.4	0.13
Zhang2012	[10]	0.05-10.5k	40	2.9	2.2	1	12.1	0.13
This work 2015		110-9.7k	52	4.27	4.7	1	5.2	0.13

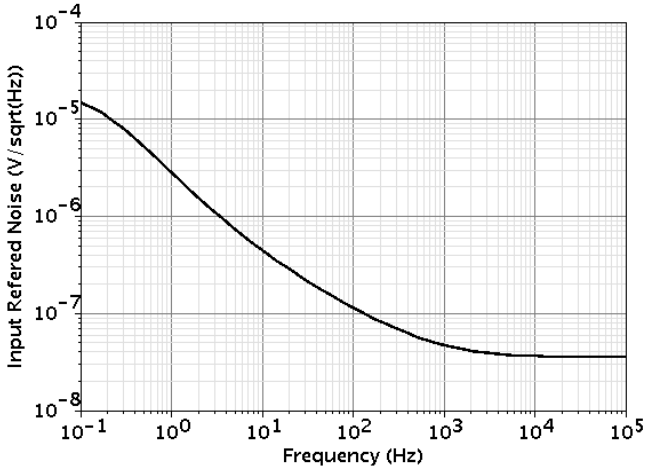

***Figure (7):** The input-referred voltage noise spectrum*

4. Conclusions:

The flipped voltage follower cell is used to build a gm-cell with effective transconductance Gm independent of the bias current. Using this gm-cell a low-voltage low-power low-noise amplifier suitable for neural recording has been designed. The amplifier uses the active low frequency suppression topology to reject DC offset, which decreases the area. The amplifier has an input referred voltage noise of 4.7 μV_{rms}. It consumes 5.2 µW. it is able to operate at 1V supply voltage. Its bandwidth is 110-9.9k Hz. The NEF is 4.27.

References:

[1] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 958-965, 2003.

[2] B. Gosselin*, et al.*, "A low-power integrated bioamplifier with active low-frequency suppression," *Biomedical Circuits and Systems, IEEE Transactions on,* vol. 1, pp. 184-192, 2007.

[3] H. Wu and Y. P. Xu, "A 1v 2.3uw biomedical signal acquisition ic," in *2006 IEEE International Solid State Circuits Conference-Digest of Technical Papers*, 2006, pp. 119-128.

[4] R. G. Carvajal*, et al.*, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS,* vol. 52, 2005.

[5] M. Steyaert, "A micropower low-noise monolithic intrumention amplifier for medical purposes," *IEEE J. Solid-State Circuits,* vol. 22, pp. 1163-1168, 1987.

[6] W. Wattanapanitch*, et al.*, "An energy-efficient micropower neural recording amplifier," *Biomedical Circuits and Systems, IEEE Transactions on,* vol. 1, pp. 136-147, 2007.

[7] H. Rezaee-Dehsorkh*, et al.*, "Analysis and design of tunable amplifiers for implantable neural recording applications," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on,* vol. 1, pp. 546-556, 2011.

[8] V. Majidzadeh*, et al.*, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *Biomedical Circuits and Systems, IEEE Transactions on,* vol. 5, pp. 262-271, 2011.

[9] C. Qian*, et al.*, "A micropower low-noise neural recording front-end circuit for epileptic seizure detection," *Solid-State Circuits, IEEE Journal of,* vol. 46, pp. 1392-1405, 2011.

[10] F. Zhang*, et al.*, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *Biomedical Circuits and Systems, IEEE Transactions on,* vol. 6, pp. 344-355, 2012.